10/091792
03/06/02

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10091792	03/06/2002	338	308	2832	

**APPLICANTS: Huber Louis; Shoshani Ziv;

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A DIV OF 09/811,844 03/19/2001

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		P04870US1
Verified and Acknowledged Examiners's intials			

TITLE : Method for manufacturing a power chip resistor

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg. / Print Fig.
		Primary Examiner		
☐ TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)